Hardware Design

Tutorial 7

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Conceptual Questions

Fill the following table

9. For these mem technologies:

	DRAM cell	SRAM Cell	D-latch
# of Transistors and capacitors	1T1C	6T	8T
Refresh?	Y	N	N
Principles	Charge sharing	Positive feedback	nand

Conceptual Questions

- What is the role of the capacitor in DRAM?
  - A. It acts as a gate.
  - B. None of the options.
  - C. Store "binary value".
  - D. Provide isolation against the "binary value".

- What happens to DRAM cells over time?
  - A. Charge starts leaking over time.
  - B. All of the options.
  - C. The cells evolve to store even more charge over time.
  - D. Charge gets overloaded above maximum rated values.

Conceptual Questions

- What is a fundamental problem with any kind of memory technology?
  - A. It does not support reads and writes.
  - B. It can be big or fast, but not both.
  - C. It always provides extremely low bandwidth.
  - D. It does not store binary data.

Question 1

MEMORY HIERARCHY AND CPU PERFORMANCE

Calculating Cache Performance

- Assume the **miss rate of an instruction cache is 2%** and the **miss rate of the data cache is 4%.** If a processor has a **CPI of 2 without any memory stalls** and the **miss penalty is 100 cycles for all misses**, determine how much faster a processor would run with a perfect cache that never misses. Assume the frequency of all loads and stores is 36%.
- $IRON\ LAW: ExecTime = IC \times CT \times CPI$
- $Speedup = \frac{Perf_{fast}}{Perf_{slow}} = \frac{ExecTime_{slow}}{ExecTime_{fast}} = \frac{ExecTime_{inst} + ExecTime_{instmiss} + ExecTime_{datamiss}}{ExecTime_{inst}}$
- Assume $IC = I$
- $ExecTime_{slow} = I \times CT \times 2 + 2\% \times I \times CT \times 100 + 36\% \times 4\% \times I \times CT \times 100$
- $ExecTime_{slow} = 2\ ICT + 2ICT + 1.44ICT = 5.44ICT$
- $ExecTime_{fast} = I \times CT \times 2 = 2ICT$
- $Speedup = \frac{Perf_{fast}}{Perf_{slow}} = \frac{ExecTime_{slow}}{ExecTime_{fast}} = \frac{5.44ICT}{2ICT} = 2.72$

Q1 Answer

- Th e number of memory miss cycles for instructions in terms of the Instruction count (I) is
- Instruction miss cycles = I x 2% x 100 = 2.00 x I
- As the frequency of all loads and stores is 36%, we can find the number of memory miss cycles for data references:
- Data miss cycles = I x 36% x 4% x 100 = 1.44 x I

The total number of memory-stall cycles is 2.00 I + 1.44 I = 3.44 I. This is more than three cycles of memory stall per instruction. Accordingly, the total CPI including memory stalls is 2 + 3.44 = 5.44. Since there is no change in instruction count or clock rate, the ratio of the CPU execution times is

$$\frac{\text{CPU time with stalls}}{\text{CPU time with perfect cache}} = \frac{\text{I} \times \text{CPI}_{\text{stall}} \times \text{Clock cycle}}{\text{I} \times \text{CPI}_{\text{perfect}} \times \text{Clock cycle}} = \frac{\text{CPI}_{\text{stall}}}{\text{CPI}_{\text{perfect}}} = \frac{5.44}{2}$$

The performance with the perfect cache is better by $\frac{5.44}{2} = 2.72$.

Question 2

CALCULATING AVERAGE MEMORY ACCESS TIME

Calculating Average Memory Access Time

- Find the AMAT for a processor with a 1 ns clock cycle time, a miss penalty of 20 clock cycles, a miss rate of 0.05 misses per instruction, and a cache access time (including hit detection) of 1 clock cycle. Assume that the read and write miss penalties are the same and ignore other write stalls.
- $IRON\ LAW$: $ExecTime = IC \times CT \times CPI$
- $AMAT = \frac{ExecTime_{mem}}{IC_{mem}} = Time\ for\ a\ hit + MissRate \times MissPenalty$
- Time for a hit per instruction: $CT_{hit} \times CPI_{hit} = 1nspc \times 1cycle$=1ns
- Time for a miss: $0.05 \times 1nspc \times 20cycles = 1ns$
- $AMAT = 1ns + 1ns = 2ns$

Answer

The average memory access time per instruction is

$$\begin{aligned} \text{AMAT} &= \text{Time for a hit} + \text{Miss rate} \times \text{Miss penalty} \\ &= 1 + 0.05 \times 20 \\ &= 2 \text{ clock cycles} \end{aligned}$$

or 2 ns.