KING'S College LONDON

Hardware Design

Tutorial 5

Instructor: Dr. Haiyu Mao
TA: Zihao Pu

27.02.2026

Question 1

MICROARCHITECTURE – MULTI-CYCLE SYSTEM FAILURE ANALYSIS

Microarchitecture - malfunctions

Suppose one of the following control signals in the multicycle MIPS processor has a stuck-at-0 fault, meaning that the signal is always 0, regardless of its intended value. Which of the following supported instructions would malfunction? Why?

(a) MemtoReg

(b) ALUOp[0]

(c) PCSrc

Supported Instructions:

- R-type
- LW
- SW
- BEQ
- ADDI
- J

Table 2: ALUOp Encoding Table

***ALUOp* encoding**

ALUOp	Meaning
00	add
01	subtract
10	look at `funct` field
11	n/a

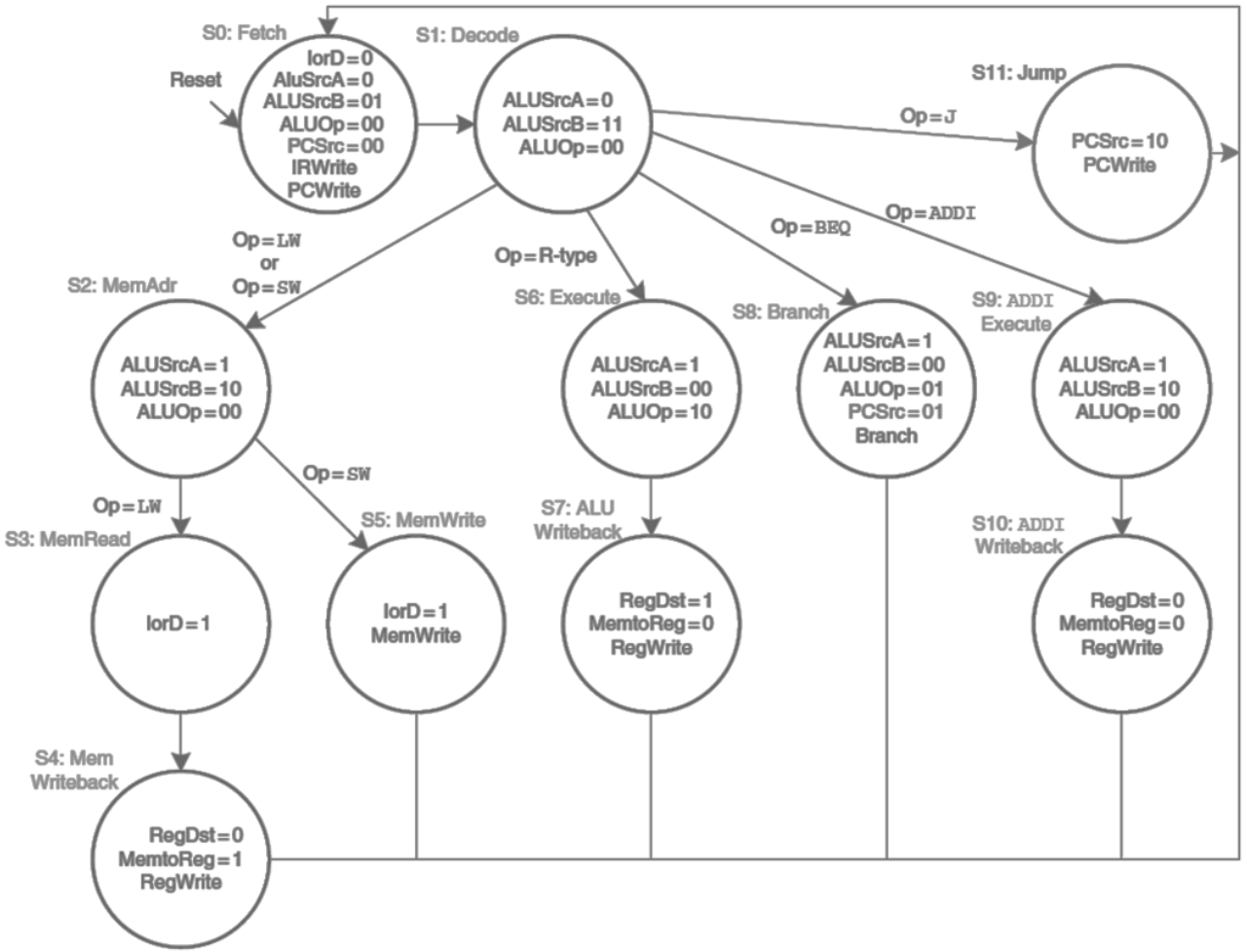
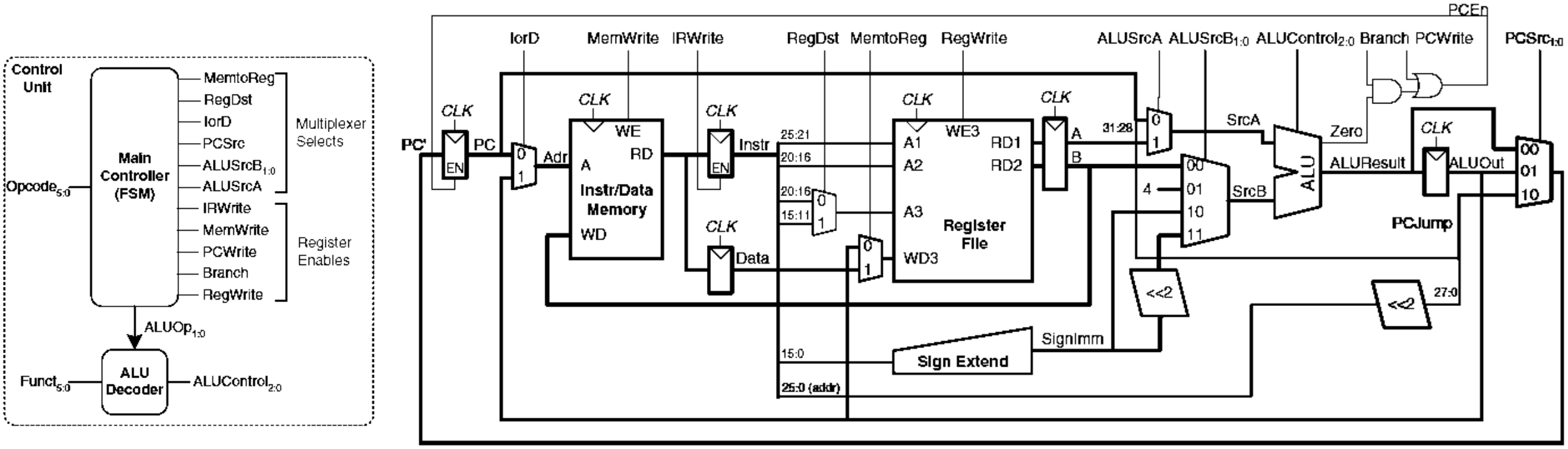


Figure 1: Multi-cycle Processor FSM State Transition Diagram

Microarchitecture - malfunctions

Supporting Figures:
Figure 2: Multi-cycle MIPS Processor Architecture



Q1 Answer

- A) lw
- B) beq
- C) beq, j

Recap: Performance Evaluation

Iron Law of Processor Performance: The performance of a processor is the time it takes to execute a program

$$\frac{Time}{Program}$$

CPI: Cycle per Instruction, determined by microarchitecture.
CT: Cycle Time, or the time spent per cycle. Usually determined by technology. Clock Rate is the inverse of cycle time.
IC: Instruction Count. The total number of instructions of a program. CISC ISA usually uses fewer instructions.

$$ExecTime = \frac{Time}{Program} = IC \times CT \times CPI$$

For execution time $ExecTime$, lower is better.
The other way to examine performance of a processor is:

$$Performance = \frac{1}{ExecTime}$$

Where higher is better.

Question 2

MICROARCHITECTURE – PERFORMANCE ANALYSIS

Evaluate Performance

Consider three different processors, P1, P2, and P3, executing the same instruction set. P1 has a 3 GHz clock rate and a CPI of 1.5. P2 has a 2.5 GHz clock rate and a CPI of 1.0. P3 has a 4.0 GHz clock rate and has a CPI of 2.2.

a. Which processor has the highest performance expressed in instructions per second?
b. If the processors each execute a program in 10 seconds, find the number of cycles and the number of instructions.
c. We are trying to reduce the execution time by 30%, but this leads to an increase of 20% in the CPI. What clock rate should we have to get this time reduction?

Q1 Answer

a.

performance of P1 (instructions/sec) 3 x 10^9/1.5=2x10^9
performance of P2 (instructions/sec) 2.5x10^9/1.0=2.5x10^9
performance of P3 (instructions/sec) 4x10^9/2.2=1.8x10^9

P2 is the best-performing processor

b.

cycles(P1) $=10 \times 3 \times 10^9 = 30 \times 10^9$
cycles(P2) $=10 \times 2.5 \times 10^9 = 25 \times 10^9$
cycles(P3) $=10 \times 4 \times 10^9 = 40 \times 10^9$

IC(P1)$=\frac{30\times10^9}{1.5} = 20 \times 10^9$
IC(P2)$=\frac{25\times10^9}{1} = 25 \times 10^9$
IC(P3)$=\frac{40\times10^9}{2.2} = 18.18 \times 10^9$

c.

Reduce ExecTime by 30%, CPI increase 20%

Knowing ExecTime=IC x CT x CPI, where IC is a constant

$$CT = \frac{ExecTime}{IC \times CPI}$$

$$\frac{CT_{new}}{CT} = \frac{ExecTime_{new}}{IC \times CPI_{new}} \times \frac{IC \times CPI_{old}}{ExecTime_{old}}$$

$$= \frac{ExecTime_{new}}{ExecTime_{old}} \times \frac{CPI_{old}}{CPI_{new}} = \frac{0.7}{1.2} = 0.5833$$

Since clock rate is inverse of cycle time:
Clock Rate (P1) = 3GHz/0.5833=5.14GHz
Clock Rate (P2) = 2.5GHz/0.5833=4.28GHz
Clock Rate (P3) = 4.0GHz/0.5833=6.75GHz